REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The non-final Office Action dated May 27, 2009 has been received and its contents carefully reviewed.

Claims 1-31 are currently pending, of which claims 8-31 are withdrawn from consideration. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, claims 1-3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Komiya (U.S. Patent Application Publication No. 2002/0158587 in view of Kochever (U.S. Patent No. 2890332), and claims 4-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Komiya in view of Kocherver, further in view of Morosawa (U.S. Patent Application Publication No. 2006/0139251). These rejections are respectfully traversed and reconsideration is requested.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "... a bias switch, connected between the N-1th compensation voltage supply line and a control terminal of the driving TFT connected to the Nth compensation voltage supply line to apply a bias voltage to the driving TFT connected to the Nth compensation voltage supply line when a scan pulse is supplied to the N-1th gate line, wherein the bias switch is controlled by the scan pulse supplied to the N-1th gate line...." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 1, and claims 2-7, which depend therefrom, are allowable over the cited references.

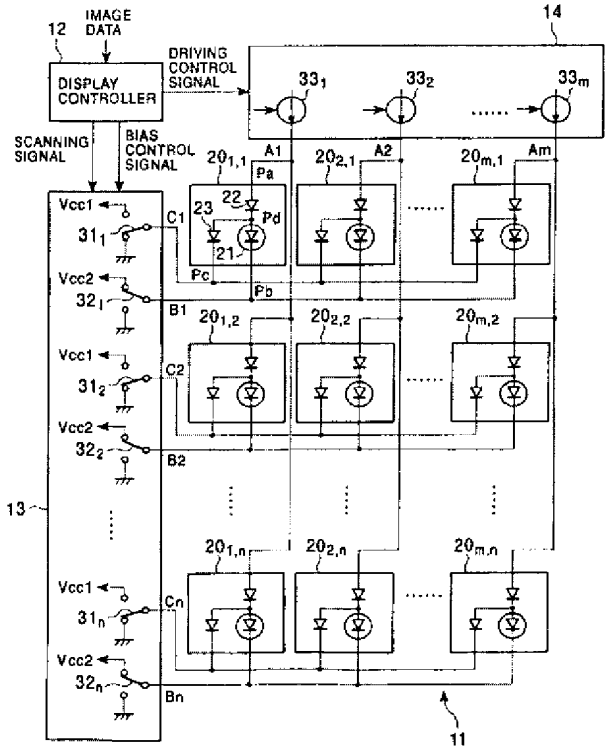
On page 3 of the Office Action, the Examiner asserts that Komiya teaches an electro-luminescence display including: connection between N-1th compensation voltage supply line (e.g., second VEE line) and a control terminal of the driving TFT and a control terminal of the driving TFT (e.g., TFT2) connected to the Nth compensation voltage (e.g., VEE line of second row), to apply a voltage to the driving TFT connected to the Nth compensation voltage supply line (e.g., TFT2) when a scan pulse is supplied to the N-1th gate line, wherein the bias switch is controlled by the scan pulse supplied to the N-1 gate line (e.g., gate line 1, see Fig. 5). Also, the Examiner asserted that Komiya does not teach a bias switch but rather uses a conventional switch to operate the compensation mechanism between the adjacent gate

lines and the pixel structures (see Fig. 5). To cure this deficiency, the Examiner asserts that Kochevar teaches a bias switch as a function circuit component having the capability to be adapted by any electric system (i.e. the demonstration of the working parameter of the bias switch and its implementation within a display system as a complete component) (see Kochevar Fig. 1, Co,, 1, lines 15-45). And also, on page 4 of the Office Action the Examiner asserts that Komiya and Kochevar teaches wherein the bias switch (Okuda 31) includes a control terminal connected to the N-1th gate line e.g., gate line 1).

However, there are great differences between the bias switch of the claimed invention and those of Okuda, Kochevar and Komiya.

At first, the bias switch (SW) of the claimed invention is controlled by a scan pulse supplied to the N-1th scan line. On the other hand, each of reverse bias switches (31_1-31n) of Okuda is controlled by a bias control signal from a display controller (12) as shown in Fig. 3 and the description related to Fig. 3 of Okuda. Accordingly, the reverse bias switches of Okuda fail to disclose the bias switch of the claimed invention.

[Fig. 3 of Okuda]



The switch TFT3 of Komiya also fails to disclose the bias switch (SW) of the claimed invention is controlled by a scan pulse supplied to the N-1th scan line because the switch TFT

of Komiya has a gate which is not controlled by the gate line 1 but the discharge gate line 1, as shown in Fig. 5of Komiya.

[Fig. 5 of Komiya]

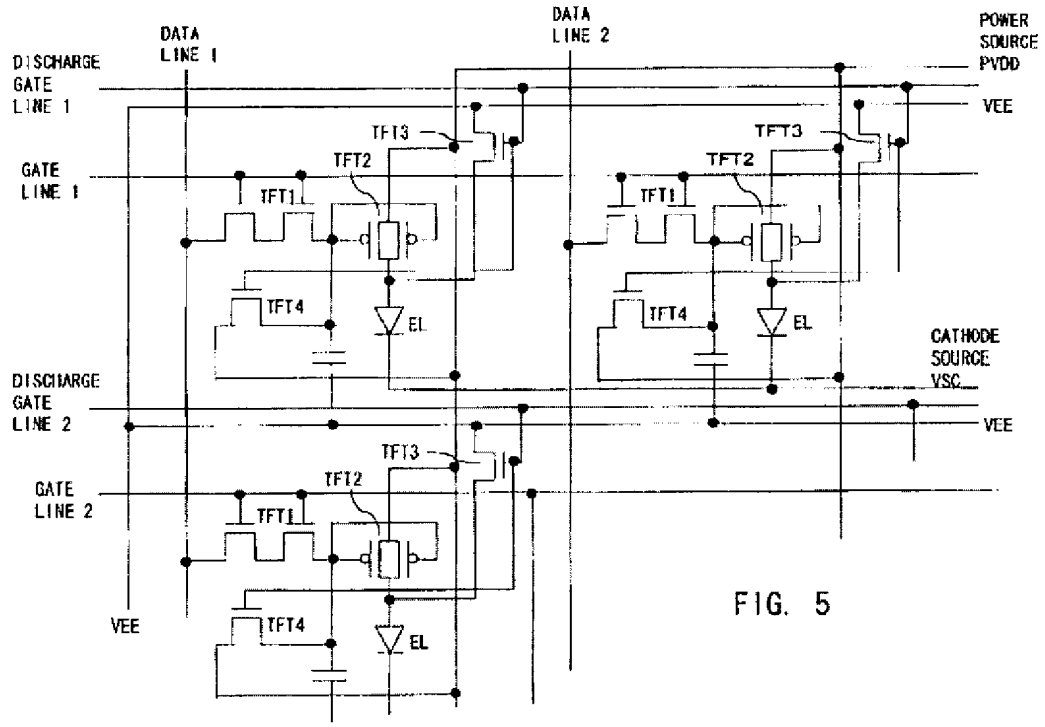


FIG. 5

The bias switch of Kochevar provides a bias voltage which is independently variable for two sets of conditions. However, the bias switch is applicable to a cathode ray tube (see Kochevar, column 1, lines 17-19). In general, the technical principle of the cathode ray tube display is different from that of the claimed invention because the claimed invention relates an EL display. Accordingly, although Kochevar is combined with the Komiya, it is impossible to obtain the construction of the claimed invention because none of the cited references teach the bias switch of the claimed invention controlled by a scan pulse supplied to the N-1th scan line.

Secondly, the bias switch (SW) of the claimed invention is connected between the N-1th compensation voltage supply line (VSLn-1) and a control terminal of the driving TFT (T2) connected to the Nth compensation voltage supply line (VSLn). On the other hand, the switch TFT3 of Komiya is connected between the compensation voltage line (VEE) and EL element (EL). Accordingly, Komiya fails to disclose the connection of the claimed invention

between the N-1th compensation voltage supply line and a control terminal of the driving TFT connected to the Nth compensation voltage supply line

Also, the reverse bias switch (e.g. C1) of Okuda is connected between the reverse bias line (C1) and a potential Vcc1 or a ground potential. That is, the reverse bias switch (e.g. C1) is not connected to any control terminal of the driving TFT. Accordingly, the reverse bias switches of Okuda are different from the bias switch the claimed invention. Komiya also fails to disclose the bias switch connected between the N-1th compensation voltage supply line (VSLn-1) and a control terminal of the driving TFT (T2) connected to the Nth compensation voltage supply line (VSLn).

Lastly, the bias switch (SW) of the claimed invention supplies a bias voltage from the N-1th compensation voltage supply line (VLSn-1) to the driving TFT connected to the Nth compensation voltage supply line when a scan pulse is supplied to the N-1th gate line because the scan pulse supplied to the N-1th gate line is also supplied to the bias switch. On the other hand, the reverse bias switch selectively supplies one of the potential Vcc1 and the ground potential to the reverse bias line (C1). Accordingly, Okuda fails to disclose the reverse bias switches supplying a bias voltage from the N-1th compensation voltage supply line to the driving TFT connected to the Nth compensation voltage supply line. Komiya also fails to disclose the bias switch described in the claimed invention.

Accordingly, there is not any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Komiya using the bias circuit of Kochevar or the reverse bias switch of Okuda.

Accordingly, Applicants respectfully submit that claim 1, and claims 2-7, which depend from claim 1 are patentable over Komiya, Kochevar, Okuda and Morosawa because none of Komiya, Kochevar, Okuda and Morosawa teaches, either expressly or inherently, at least these features of the claimed invention.

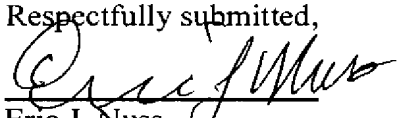
Applicants believe the application is in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

Dated: August 19, 2009

Respectfully submitted,



Eric J. Nuss
Registration No.: 40,106
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant